ABSTRACT

A system for and a method of integrating SRAM cells and flash EPROM cells onto a single silicon substrate includes an area on the silicon substrate where a local oxidation of silicon (LOCOS) isolation technique is implemented and another area on the same silicon substrate where a shallow trench isolation (STI) technique is implemented. Further, this system and method also include flash EPROM cells implemented within the area of the substrate utilizing the LOCOS isolation technique and SRAM cells implemented within the area of the substrate utilizing the STI technique. Preferably, the LOCOS isolation technique is first implemented to define a flash area of the silicon substrate on which the flash EPROM cell is implemented. Before the LOCOS isolation technique is implemented, an SRAM area is masked. After the LOCOS isolation technique has been fully implemented, the flash area is then preferably masked and the STI technique is implemented in order to define the SRAM area of the silicon substrate on which the SRAM cell is implemented. After the STI technique is implemented, the flash EPROM and the SRAM cells are preferably formed. Thus, the SRAM cells and the flash EPROM cells are both implemented on the common silicon substrate, but yet are appropriately isolated from each other, as well as from other additional devices which may be further implemented on the same silicon substrate, while providing the advantages of respective isolation schemes for the two cells.